High Energy
High Intensity
Hadron Beams

Proceedings of Workshop on “Trajectory and Beam position measurements using digital techniques” 22.-23. June 2004

Edited by K. Wittenburg[1]

1) DESY, Hamburg, Germany

Abstract

This report contains the final proceedings of the 1st meeting in the framework of the CARE-HHH-ABI networking, held 22.-23. June 2004 in Aumuehle, with the subject: "Trajectory and Beam position measurements using digital techniques".

Proceedings of the 1st meeting in the framework of the CARE-N3-ABI networking

CARE-Conf-04-024-HHH

"*Trajectory and Beam position measurements using digital techniques*"

Aumühle, 22.-23. June 2004

A. Peters, H. Schmickler, M. Wendt, K. Wittenburg

Introduction to the meeting

This meeting is the first of a future series of network meetings in the framework of the CARE-N3-ABI networking. **ABI** (**A**ccelerator **B**eam **I**nstrumentation) is a Work package of **HHH** (**H**igh energy **H**igh intensity **H**adron beams) in the framework of CARE (**C**oordinated **A**ccelerator **R**&D in **E**urope) N3 (Networking Activities). CARE is supported by the European Community EU (FP6 Research Infrastructure Action).

The aim of this workshop was to understand specific problems of implementing new digital technologies for beam orbit and position measurements in hadron machines. The new digital methods have already been successfully implemented in various synchrotron light sources. In these applications submicron resolution and long-term stability over days, even independent of seasonal changes, are the most important design criteria. The digital solutions profit from the electron beams being fully relativistic (no change of revolution frequency) and from the very small variation of bunch intensities. Proposing similar digital technologies for hadron machines confronts the designers with several additional problems:

- A large variation in bunch intensities and filling patterns
- Change of harmonic numbers with beam in the machine
- Varying revolution frequency
- Demands for multi-bunch and multi-turn data

The purpose of the workshop was also to bring together people with experience from digital orbit systems in Synchrotron Light sources and people who intend to implement this technology in hadron machines (GSI and CERN). During the three half-day sessions the following was done:

- review of performance and design issues in light source implementation,
- review of specifications for hadron machines,
- attempt of technical solutions and proposal of test measurements.

The workshop had found interest in related industrial partners and those visited the workshop at their own cost. About 20 people from the following labs participated: ESRF, PSI, DESY, GSI, CERN, COSY, TU Darmstadt (plus companies: Bergoz, France and Instrumentation Technologies – "i-tech", Slovenia).

The main focus of this meeting laid on interactive discussions between the invited specialists to get a better understanding and a guideline for solutions of the specific problems in hadron accelerators, in particular in the LHC preaccelerators and for the GSI/FAIR project. Therefore these proceedings will summarize the discussions, while the presentations act more as an incitation for the adjacent sessions.

Agenda of the meeting:

a) First half day:

0) Welcome; Kay Wittenburg, 5 min
1) CARE-N3 networking; H.Schmickler, 10min
2) Overview of the existing digital receiver systems; M.Wendt, 20 mins
3) The proposed DSP-system for BNL and CERN low level Rf control; H. Schmickler, 15 min
4) 30 min Discussion
5) Detailed description of PSI implementation including specs (bandwidth, noise…) Patrick Pollet, Thomas Schilcher , 30 min talk, 30 mins discussion
6) round table; experience with existing systems with contributions from ESRF and SPEAR3.
   Discussion leader: Manfred Wendt

b) Second half day:

1) Specific requirements of hadron machines: CERN-PS -frequency range, frequency sweep, bunch "gymnastics", intensity variation: U.Raich, J.Belleman. 30 mins talk, 30 mins discussion
2) GSI-FAIR, same as above, A:Peters et al. 30 mins talk, 30 mins discussion
3) Discussion: Upgrade wishes of other existing installations
4) Presentation of commercially available new products; today and future: R.Ursic and J..Bergoz followed by a first discussion

c) Third half day

1) Round table:
   What does the hardware do in this case of the present digital receivers?
   Description of main chips. What alternatives are on the market?
   Where are the shortcomings of the presently available commercial solutions.
   What has to be done to overcome this. Outlook to other planed ideas or systems.
   Discussed topics:
   1) Hardware; ADCs, Digital Receivers, FPGAs, DSPs
   2) Different Front Ends; Analogue and Digital Signal Preparation
   3) Algorithms for Data Analysis
   Discussion leader H.Schmickler
   This round table gives the possibility for **SHORT** prepared contributions. The discussion leader will contact individual participants in order to have something prepared.
2) Brainstorming on subjects for Upcoming CARE N3 ABI events
3) Round Table: What are the next steps to be done in concrete terms:
   Road map to CERN-PS and GSI-FAIR system,
   Discussion leader: A.Peters

Summary of 1st first half day

After the welcome at the meeting by K. Wittenburg and an introduction to the CARE HHH networking by H. Schmickler, M. Wendt gave an overview over the existing implementations of digital receivers in accelerator Beam Position Monitor (BPM) Systems:

Examples of Existing Digital BPM Systems:

by M. Wendt; DESY, Hamburg

Contents:

- INTRODUCTION TO BPM SIGNAL PROCESSING
- DIGITAL BPM RECEIVER FOR THE SLS
- DIGITAL BPM SIGNAL PROCESSING FOR THE FNAL RECYCLER RING
- OTHER EXAMPLES OF DIGITAL BPM SIGNAL PROCESSING
- ROUND TABLE DISCUSSION

Introduction to BPM Signal Processing

The core hardware (Fig. 1) of a BPM system consists out of:

- BPM pickup station, which usually delivers beam position and intensity dependent signals from 4 symmetrically arranged electrodes.
- BPM read-out electronics, which processes and normalizes the electrode signals toward horizontal and vertical beam position information; either in an analog or digital or mixed way.

It should be considered, that the BPM hardware does not know that it is a digital or analog...(!). The task of the BPM signal processor is twofold:

1. Normalization; Get rid of the beam intensity by normalization, e.g.:

   $V_{Up\text{-}elec} = s(x,y)\, Z(\omega)\, I_{beam}(\omega)$; $V_{Down\text{-}elec} = s(x,-y)\, Z(\omega)\, I_{beam}(\omega)$ with

   $$\text{vert. beam position} = f\left(\frac{V_{UP-elec} - V_{DOWN-elec}}{V_{UP-elec} + V_{DOWN-elec}}\right) = f\left(\frac{\Delta}{\Sigma}\right)$$

   or

   $$= f\left(\frac{V_{UP-elec}}{V_{DOWN-elec}}\right)$$

   vert. beam position = $f(x,y) \approx f(y)$

   The sensitivity $s(x,y)$ depends on the beam-to-electrode distance and the cross-section geometry of the BPM pickup

2. Signal Processing in terms of signal shaping, filtering, amplification and acquisition towards beam displacement information of highest possible resolution.

An overview of (analog) BPM signal processing techniques was given by G. Vismara (Ref. 1. and 2.).

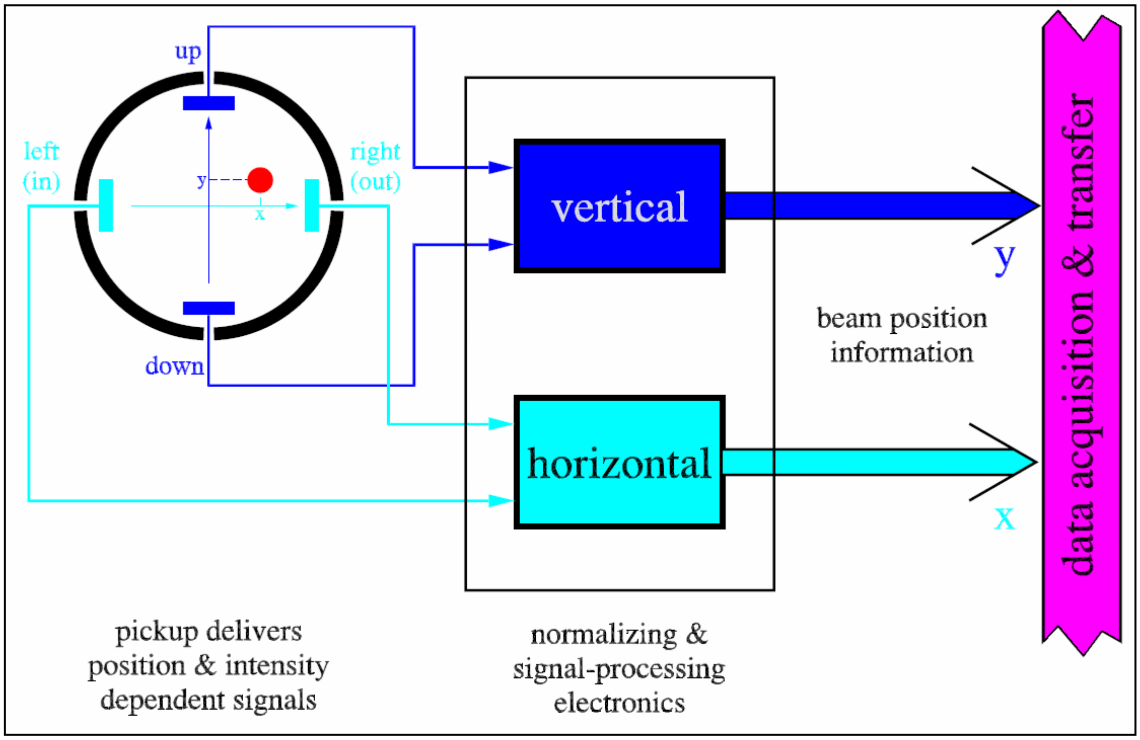


Fig. 1: Core hardware of a BPM

Definition:

Let us define a digital BPM signal processor as a hardware unit where parts or all of the signal processing and normalization is performed digitally. The design considerations for the BPM instrumentation varies among the different labs and their accelerator projects:

- Stimulus signals of hadrons (p, $\bar{p}$ or ions) have a rather long bunch length and may be non-relativistic.
- Attention has to be paid to the type of BPM pickup, e.g. broadband (button, stripline) or resonant type (dipole mode cavity) and it's cross-section geometry. In lepton (e^+, e^-) storage rings the pickup electrodes cannot be arranged in the horizontal plane because of the interference with the synchrotron light.
- The BPM signals of linear accelerators or transport lines have no revolution harmonics ($n \cdot f_{rev}$), thus require a single-pass time domain approach.
- In storage ring colliders the BPM system may have to manage signals from two beams in the same vacuum chamber, e.g. p and $\bar{p}$ in the Tevatron, p and e in the HERA interaction regions.
- The measurement (or integration) time of the signal processing system determines the type of BPM operation, e.g. bunch-by-bunch, turn-by-turn or a high resolution multiturn measurement in ring accelerators; single bunch or bunch train integrated measurements in linear accelerators. The resolution of a BPM system, as most important system characteristic, depends highly on this parameter!

- Other aspects of BPM signal processors are the kind of data transfer, synchronization and triggering issues and the way (synchron or asynchron) the signal sampling is performed.
- Radiation issues in large storage rings have to be considered and may result in long signal cables between pickup electrodes and BPM read-out electronics.

The Digital BPM Receiver of the SLS

The Swiss Light Source (SLS) is a 2.4 GeV, 288 m long circumference 3rd generation synchrotron light source. It is the first accelerator equipped with a BPM signal processing system based on the digital receiver technology (Figure 2). The primary purpose is it's implementation in a fast orbit feedback system. A resolution of < 1 μm in the 2 kHz bandwidth feedback-mode was achieved.

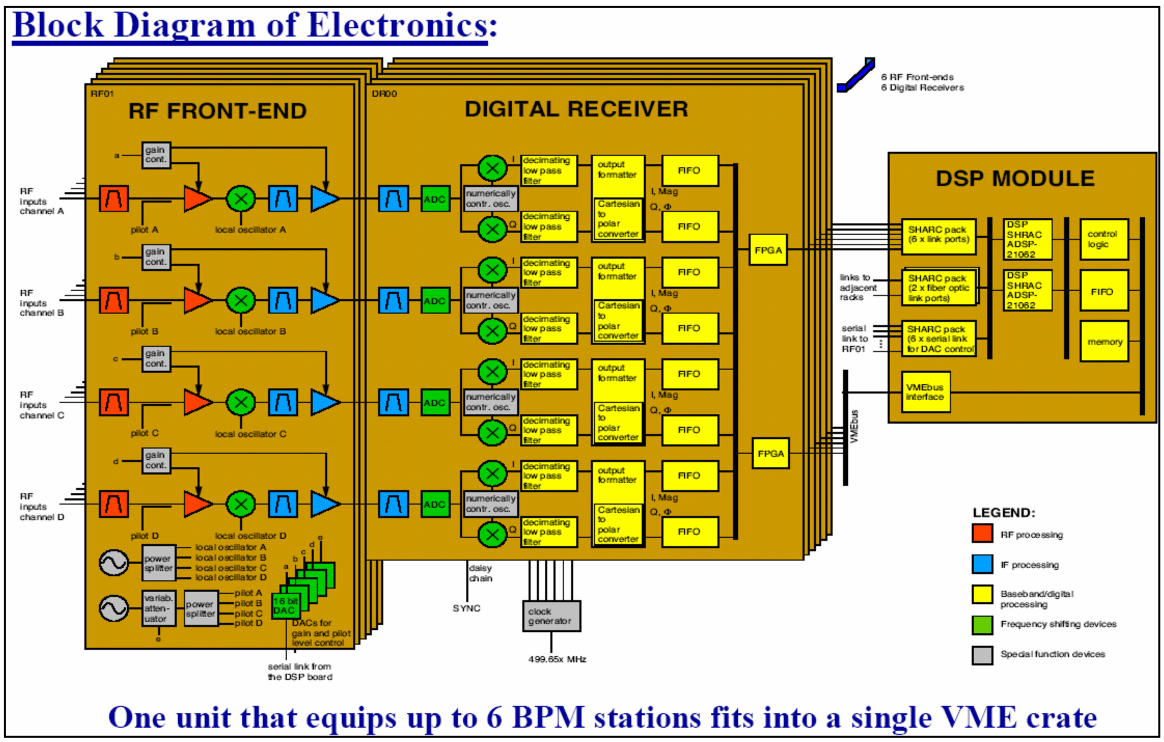


Fig. 2: Digital receiver at SLS; block diagram of electronics

Key features:

- BPM system acquiring the signals of 72 button type BPM pickups.
- The signal processor is based on a 4-channel superhetorodyne receiver with digital AM quadrature demodulator (so-called digital receiver).
- Key components are: 12-bit, 41 MSPS, 100 MHz BW ADC (Analog Devices AD9042) and a direct down converter (DDC) (Intersil HSP50214B).
- Programmable bandwidth DC...500 kHz.
- On-line calibration by feeding a 498 MHz "pilot signal".

The rf-receiver is tuned to the fundamental f_{rf} = 500 MHz and down-converts the electrode signal to f_{if} =36 MHz (5 MHz BW).

Digital BPM Signal Processing for the FNAL Recylcer Ring

237 capacitive split-plate BPM pickup's with a new BPM read-out system are used to acquire the beam orbit of bunched and un-bunched(!) p- and p^bar-beams in the FNAL recycler ring. Due to the time critical mission a commercial VME-based digital signal processor (Echotek GC-814) was chosen in favor to an VXI-board in-house development, based on the digital low-level rf processing system.

Features:

- Beam position measurement of 2.5 MHz bunched and un-bunched beams with varying barrier buckets (679...1132 ns).
- 6 different signal processing modes: 2.5 MHz averaging, 2.5 MHz bunch-by-bunch, 2.5 MHz narrow band, un-bunched average, un-bunched head/tail and 89 kHz narrow band.
- Hardware (Figure 3): Split-plate BPM pickup, analog differential receiver/filter module, 8-channel 80 MSPS DDC VME module.
- A position resolution of ± 10 μm in a 30 dB dynamic range was achieved.

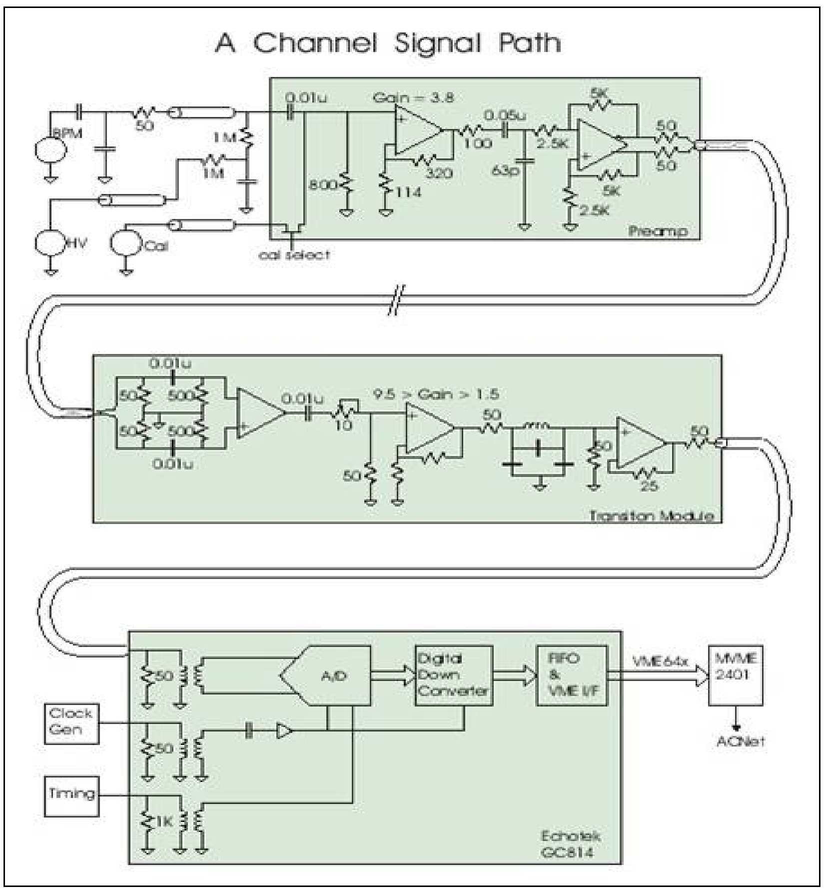


Fig. 3: Hardware of the FNAL BPM system

Other Examples of Digital BPM Signal Processing

NSRRC:
The National Synchrotron Research Center (Taiwan) has equipped it's synchrotron light source with a commercial version of the SLS digital BPM electronics (i-Tech DBPM2).
SNS:
Ring and transport-lines of the Spallation Neutron Source will be equipped with PCI-based digital front-end boards. Together with the attached, commercially developed, rf front-end (Bergoz), the digital BPM signal processing unit has to operate in different modes, resolving the beam position over a high dynamic range (approx. 60 dB) of beam intensity.
Other upcoming synchrotron light sources (like Soleil, Diamond, PETRA-III):
They will be equipped with digital BPM read-out systems, mostly commercial solutions.

As shown, digital receivers are now commercially available. The following two examples show different design philosophies:

i-Tech now offers a very complete BPM signal processing module, called Libera. It is particular suited for synchrotron light source BPM instrumentations and required no additional electronics hardware.

Echotel and other companies offer ADC/FPGA hardware units in many different hardware formats (including a 2-channel mezzanine). Additional rf front-end hardware is required, but this gives more flexibility to other (i.e. not light source related), non-standard or exotic BPM applications.

Round Table Discussion

The round table discussion in the afternoon debated on various design details on digital BPM read-out systems:

- Most, if not all applicants agreed, that the advantages of digital BPM processors are so dominant, that fully analog-based BPM systems will be an exception in the future.
- As the sampling rate of digital components (ADC's, FPGA's) was increased over the last years by nearly a factor of 10, the digital part is not anymore limited to if and demodulator sections. People agreed that new developments should try to process pickup signals directly digitally on the fundamental (carrier) system frequency.
- Today FPGA's are so powerful, that special purpose digital circuits (DDC-, receiver- or DSP-chips) are not anymore required in the digital BPM hardware.
- Nevertheless, digital systems have their own problems, some of them where mentioned in detail by R. Ursic (i-Tech) and others: Measuring the amplitude-levels with four independent channels for the four pickup electrodes is a general problem in terms of slow drifts. The pilot signal calibration realized in the SLS hardware cannot handle this problem sufficiently. A new designed matrix-switch on the commercial i-Tech Libera system will show in future BPM implementations the improvements on this problem.

More discussion was followed on the topic resolution limits due to clock jitter. This seems to be a critical issue and requires enforced engineering activities. It seems to be a general problem to handle (transmit) high-speed digital signals. Differential signal transmission (LVDS, (P)ECL) is mandatory.

The round table discussion was extended by two presentations:
E. Plouviez: Fast Digital Signal Processing of Beam Signals at ESRF
E. Plouviez gave an impressive overview of different digital signal processing techniques used at the ESRF, exploiting BPM signals for various applications (orbit measurements, orbit feedback, tune measurements, multibunch feedback, HOM detection). The individual systems are based on different hardware strategies, like FPGA's, DDC's, DSP's and fast digitizers. He first explained the general differences between these circuit philosophies with their pro's and con's. Then he explained the individual applications in detail.
H. Schmickler gave a short note on the digital BPM hardware with multiplexed electrode signals, which is under commissioning at SPEAR-3 (SLAC). This single channel hardware will handle single turn, turn-by-turn and multiturn (10000) modes by digitally processing the 16.6 MHz if of a single bunch.
This digital processing unit was added to the existing analog BPM hardware and provides a 1 μm resolution in the multiturn mode.

Summary of 2^{nd} Half Day

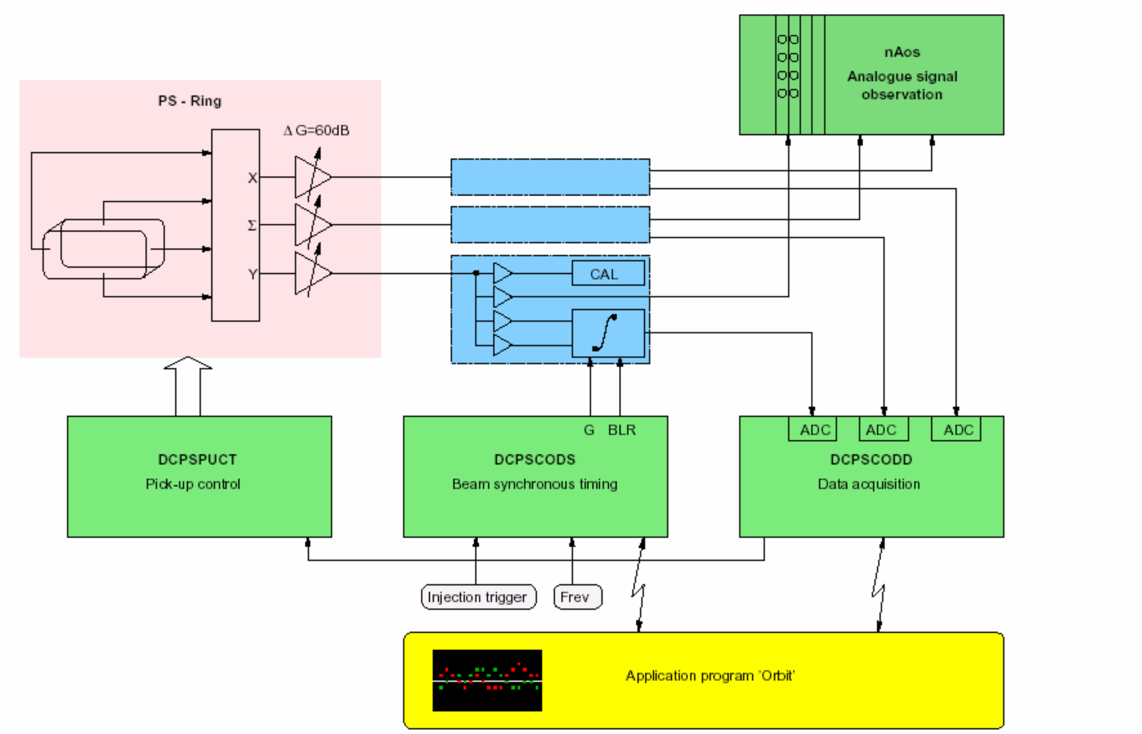
by A. Peters, GSI

The program of the second half day contains the following topics:

1. Specific requirements of hadron machines: CERN-PS -frequency range, frequency sweep, bunch "gymnastics", intensity variation: U.Raich, J.Belleman. 30 mins talk, 30 mins discussion
2. GSI-FAIR, same as above, A:Peters et al. 30 mins talk, 30 mins discussion
3. Discussion: Upgrade wishes of other existing installations
4. Presentation of commercially available new products; today and future: R.Ursic and J..Bergoz followed by a first discussion

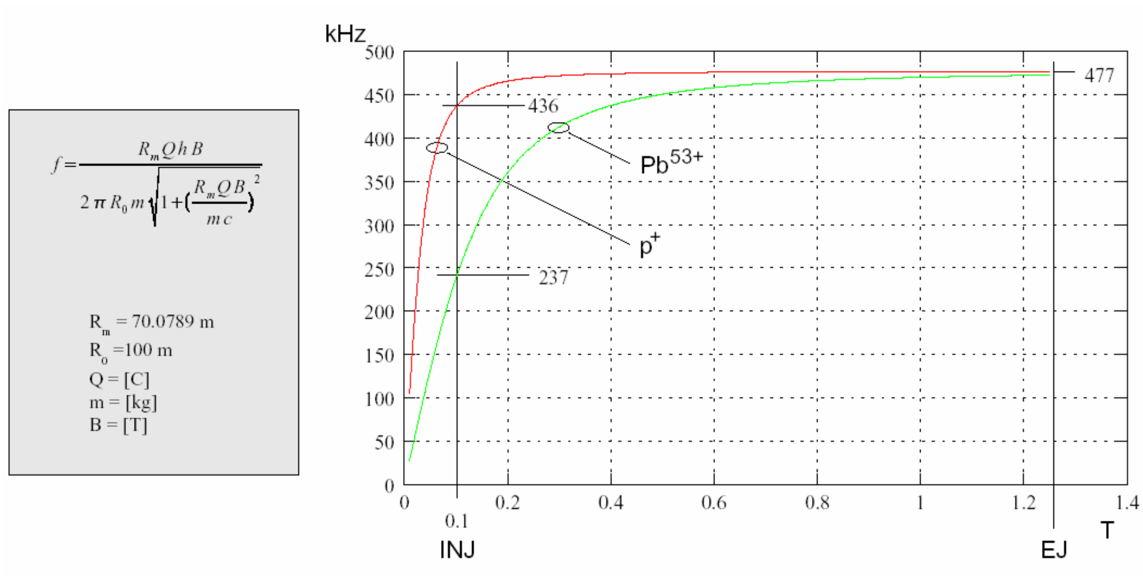
Specific requirements of hadron machines

Jeroen Belleman reports about the specific installations of the BPM systems used until today at the CERN-PS accelerator:



All these systems are mainly based on analog electronics and have to be renewed because of age and the very complex timing systems needed to extract the beam position data from the pick-up signals.

A main issue to a new – digitally based – BPM system is the varying revolution frequency and therefore varying bunch lengths and intensities:



The above given graph shows this exemplarily for the parameters of a proton and a Pb beam in the CERN-PS. Additional information are:

- Beam intensity can be from 1e9 to 7e12 q_0/b
- Bunch length can vary from 4 to 200 ns (but the PU electronics' bandwidth limits the
- minimum bunch length to 30ns)
- Number of bunches can go from 1 to 420 (but measurements beyond 21 are not needed until today)
- Bucket frequency varies from 3.4 to 10.5 MHz

Jeroen Belleman shows the various RF gymnastics which are necessary to prepare the bunch trains for the following CERN accelerators up to the LHC, which arise additional demands for a new digital BPM electronics. He summarized the necessary requirements connected to this new development for the trajectory measurement system for the CERN PS in the following table:

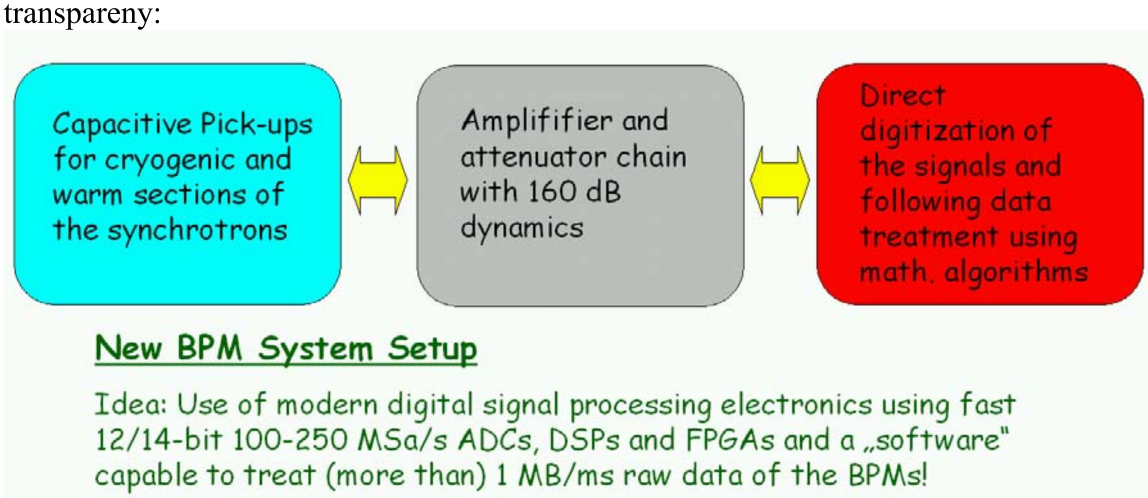
- Trajectory at injection(s), ejection(s)
- Orbit of a selected bunch everywhere else
- Mean radial position
- Single bunch, multi-turn position
- Tune?

Requirements of the GSI-FAIR accelerator complex

Andreas Peters gave a first summary of the requirements that will come up with the GSI-FAIR (**F**acility for **A**ntiproton and **I**on **R**esearch) accelerator complex, dominated by the SIS100, a fast-ramping super-conductive synchrotron of 100 Tm magnetic rigidity. He compared the parameters of the existing and future machines with those of the CERN PS and the COSY storage ring at the Forschungszentrum Jülich (see the following table) and showed that the parameters are quite equal. Based on theses similar requirements a discussion started to set up a common initiative to develop one digital system to cover all the needs for trajectory systems in hadron synchrotrons in Europe used today and in future.

Parameter	GSI SIS 18	GSI - SIS 18 Upgrade	GSI SIS 100	CERN PS	FZ-Jülich COSY
Ramp-rate (T/s)	1.3 (4.0)	4.0 (10.0)	4.0	~ 4.0	0.5 – 1.0
Max. B-Field (T)	1.8 (1.2)	1.8 (1.2)	2.0	1.3	1.7
Max. Ramp-Time (s)	1.4 (0.3)	0.45 (0.12)	0.5	0.325	2.0
Max. Cycle-time (s) (*)	1.6 (0.5)	0.5 (0.17)	0.6	1.2 – 2.4	~ some s
Frequency span (MHz)	0.8 – 5.2	0.8 – 5.2	2.2 – 5.4	3 – 10	0.4 – 1.5
Shortest bunch length (ns) (**)	~ 100	~ 50	~ 25-50	25	~ 50
Number of pick-ups (hor. / vertical)	12 / 12	12 / 12 (+4/+4)	~ 60 / 60	40 /40	31 / 31

(*) The maximum cycle time should indicate the time in the different machines where bunches exist, so that a measurement of the beam position is possible
(**) This value is necessary to understand the demanded maximum sampling speed He presented the first idea to set up such a common BPM system layout with the following transpareny:



While the pick-ups (mechanics as well as first electronics) and the amplifier chain have to be adapted to the different accelerators, the digital part based on direct digitization and data treatment with fast FPGAs and DSPs should have a common platform. A main issue will be to develop the necessary and fast mathematical algorithms to be implemented on the common HW platform, which still can be adapted to the different accelerator requirements.

Andreas Galatis from GSI, who is a doctorand at the university of Darmstadt, presented first measurements with a 100 Msample/s 12-bit 4-channel digitizer at the SIS18, the existing 18 Tm synchrotron at GSI. These data together with those taken at the CERN PS will be the basis for the first algorithm design.
Several data treating methods were discussed after this short presentation, mainly Prof. Zoubir from the TU Darmstadt, institute for signal processing, gave a lot of hints how to proceed:

- Use of FFT analysis.
- Building up a theoretical model to simulate the real bunch signals with e.g. a sum of Gausssian functions and noise terms.
- Using of several filtering techniques, e.g. median filters to find the signal slope.
- Estimation techniques to find the right integration windows.

A further need of external timing, e.g. the use of a revolution clock was also discussed as well as information about the different RF gymnastic schemes.

Commercially available new products

At the end of this session the industrial companies (Bergoz, France and Instrumentation Technologies, Slovenia) display their solutions, of main interest was the solution presented by R.Ursic. This so-called “Libera” product line was set up first with built-in digital receivers for the beam position measurements at synchrotron light facilities. The two up-coming projects in Europe (SOLEIL in France, DIAMOND in England) will be equipped with this solution, which has already the capabilities for feedbacks.
A second product line of “Libera” is now under development for hadron machines, first of all the CERN-PS accelerator:

• Analog board with four 12-bit ADC channels
• Digital board
–Virtex II Pro (FPGA fabric, Two embedded IBM PowerPC™ 405 and Eight RocketIO™ transceivers)
–SBC: Dedicated XScale® processor from Intel running Linux OS intended primarily for communication purposes
–PMC slot for additional functionality

After this presentation the necessary resolution and sampling speed of the ADCs was discussed by U.Raich from CERN and A. Peters from GSI. An open question arises, if 12 bit is sufficient for the demanded position resolution in respect to the dynamics of the input signal. This has to be studied in detail.

Summary of 3rd Half Day

by H. Schmickler, CERN

Making concrete plans

Introduction

The third half day was planned as synthesis session based on the detailed technical presentations of the day before. In particular the workshop participants wanted to produce a list of planned milestones to get to a prototype design for a digital receiver for beam position measurements on high intensity high brilliance hadron machines.

Functionality of the existing systems

At several European light sources (SLS, Diamond, SOLEIL) there exist or there are planned installations of so called "digital receivers". The basic functionality is to approach the digitizing circuits **as much as possible** to the signal source (in the ideal case just after the signal conditioning and pre-amplification circuit). In this approach all classical building blocks of a BPM system like down-mixers, paired bandpass filters, ringing filters, demodulators can be implemented as digital algorithms. The main advantage of this solutions is reduced system complexity, possibility of reconfiguration and absolute identical behaviour of all system channels.
The global tendency in the existing installations is to replace the function of very specific and specialized hardware chips (the so called digital receivers) by more general chips, which are fully user programmed (FPGAs, ASICs).
The report from the existing installations is very encouraging. The system performance is as expected and in particular the identical behavior of all channels yields a very low temperature drift of the systems.

Additional requirements of a system for hadron machines.

The basic difference of a digital receiver for an electron machine compared to a hadron machine are for two aspects:

- The revolution frequency is not constant during acceleration. The Lorentz factor of hadrons (at beam energies below the TeV) still changes significantly during acceleration, such that the particles gain speed. This means that the revolution time is non constant and that all timing signals have to be created in a dynamic way. On the contrary in all relevant electron machines the particle travel at almost the speed of light and the variation can be neglected.
- Due to the different behaviour of hadron beams, in particular due to the complete lack of synchrotron radiation and the resulting energy loss around the perimeter of the machine the phase space coordinates of each particle are preserved. This allows beam manipulations widely named "Rf gymnastics", during which hadron beams can be completely debunched and rebunched, shifted in Rf buckets or the number of bunches gets multiplied by an integer numbers (beam splitting). These Rf gymnastics are used frequently for various purposes and during these

processes any beam position measurement system must be capable of measuring the beams.

New algorithms

In order to cope with the above new demands two algorithms were identified as missing and consequently needing development:

- Auto Timing Adaptation:
  From the incoming digitized beam signals a reference signal has to be derived, which is capable to act as feedback signal to a local oscillator, which under all beam conditions is phase stable in respect to a given bunch in the machine. This algorithm is in particular very demanding during Rf gymnastics, when the definition of a particle bunch is not obvious.
- Recognition of individual bunches
  Based on the above created timing reference the signal from bunches must be obtained by integration. The implemented online algorithm has to detect the time period during which its input signal corresponds to the beam signal or during which it is part (of a moving) baseline.

Milestone definition

The following milestones were defined:

1. Until September 2004 a hardware test system should be assembled at CERN and at GSI for beam measurements. These test systems should basically consist of a preamplifier after the position pickup and a digitization chain. In case of the test system the role of the following data acquisition system was considered only as a so called "chart recorder", which should register real beam data with a maximum clock speed of 100 Msamples/s. As further objective it is agreed to take such data under the most variable beam conditions and sometimes even with the wrong parameters of the preamplifiers in order to have data representing badly adjusted signal gains.
2. The so collected data should be used for offline studies of the future algorithms. These algorithms can be implemented on any high level language on any platform.
3. The results of the algorithms as tested on the real data will be reviewed during a GSI-CERN collaboration meeting.
4. Until Spring 2005 the most promising algorithms will be selected and used as first candidates for a real time implementation onto an FPGA circuit.

Conclusion

The above work program was considered very adequate for the demanded project and the human resources were identified at GSI and CERN.

References

1) The comparison of signal processing systems for beam position monitors.
Vismara, G.; 7 p.
Report-No : CERN Geneva - CERN-SL-99-052;
CERN cern-sl/1999052

2) Signal Processing for Beam Position Monitors
Vismara, G ;
CERN-SL-2000-056-BI ;Geneva :CERN ,10 Jul 2000. -23
Pres. at: 9th Beam Instrumentation Workshop, Cambridge, MA, USA, 8 - 11 May 2000

Participants

Elettra: Mr. De Monte, Mario Ferianis
Juelich: Juergen Dietrich,
DESY: Igor Krouptchenkov, M. Wendt, Rudolf Neumann, Kay Wittenburg
GSI: Peter Forck, Andreas Peters, Piotr Kowina, Andreas Galatis
CERN: U. Raich,, J. Belleman, H. Schmickler
TU Darmstadt: Prof. Zoubir
ESRF: E. Plouviez,
PSI: Thomas Schilcher, Patrick Pollet
Bergoz : Julien Bergoz,
I-Tech: Rok Ursic, Borut Solar